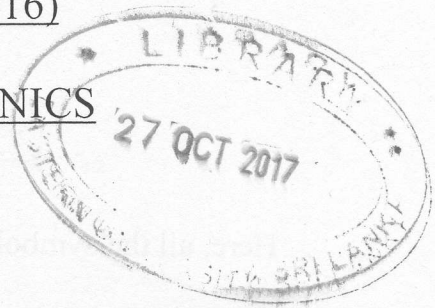


EASTERN UNIVERSITY, SRI LANKA

SPECIAL DEGREE EXAMINATION IN SCIENCE – 2010/2011

(SEPTEMBER/OCTOBER - 2016)

PH 407 ADVANCED ELECTRONICS



Time: 03 hour

Answer ALL Questions

Fig.1 shows a simple common-source amplifier circuit based on a junction field effect transistor (JFET).

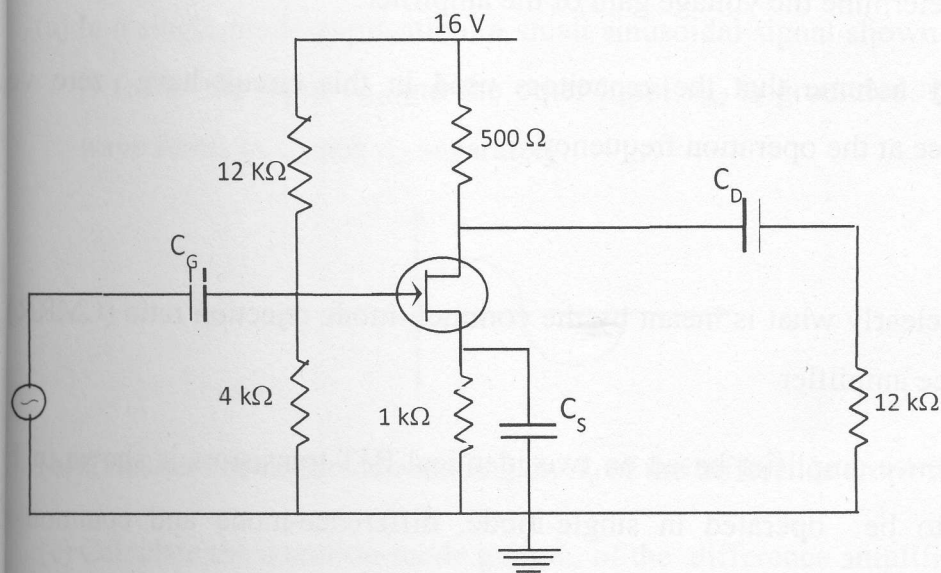
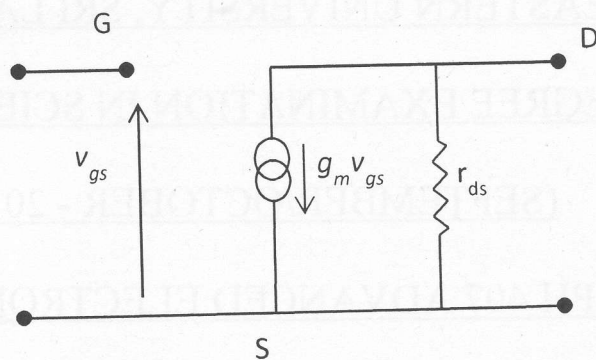


Fig.1

- (i) The voltage V_{GS} between the gate and the source is -2 V. Calculate,
 - (a) the drain current I_D and
 - (b) the voltage V_{DS} across the drain and the source.
- (ii) The small-signal equivalent circuit model for the transistor used is given below.



Here, all the symbols have their usual meanings.

- Draw a small-signal equivalent circuit model for the amplifier in Fig.
- The transistor used in this amplifier has a maximum saturation current of 12 mA and a pinch off voltage V_P of -4 V and the ac drain resistance is 12 k Ω . Estimate the small-signal transconductance g_m of the transistor.
- Determine the voltage gain of the amplifier.

You may assume that the capacitors used in this circuit have zero impedance at the operation frequency.

- Q2. Explain clearly what is meant by the common-mode rejection ratio (CMRR) of a difference amplifier.

A difference amplifier based on two identical BJT transistors is shown in Fig. 1 and is to be operated in single-mode, difference-mode and common-mode applications.

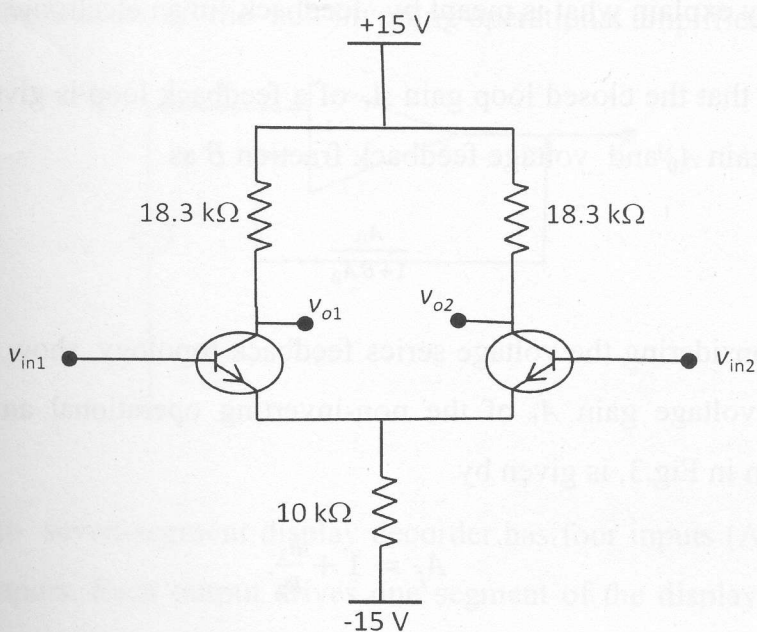
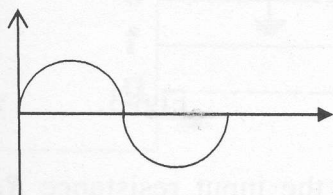


Fig. 2.

- (a) In a single-mode application, a small sinusoidal signal shown in below figure is fed to the input v_{in1} and the other input v_{in2} is grounded. Draw the output wave forms in v_{o1} and v_{o2} separately.



- (b) Calculate the difference-mode gain A_d of the difference amplifier.
 (c) Calculate the common-mode gain A_c of the difference amplifier.
 (d) Hence, estimate CMMR of the the difference amplifier.

You may find the following relations are useful.

$$A_d = \frac{R_C}{2r_e} \quad \text{and} \quad A_c = \frac{-R_C}{r_e + 2R_E}$$

Here, the symbols have their usual meanings.

- Q3. (i) Briefly explain what is meant by 'feedback' in an electronic circuit.
- (ii) Show that the closed loop gain A_f of a feedback loop is given in terms of loop gain A_0 and voltage feedback fraction B as

$$\frac{A_0}{1+BA_0}$$

- (iii) By considering the voltage series feedback topology, show that the loop voltage gain A_f of the non-inverting operational amplifier shown in Fig.3, is given by

$$A_f = 1 + \frac{R_1}{R_2}$$

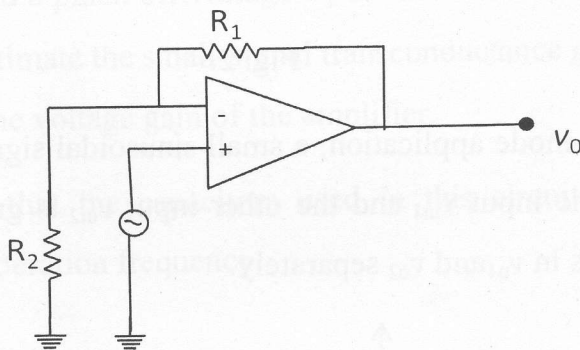


Fig. 3.

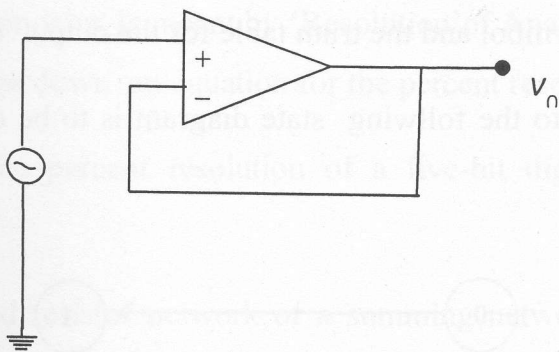
- (iv) Also, show that the input resistance R_f of the non-inverting operational amplifier circuit is given by

$$R_f = R_i(1 + BA_0),$$

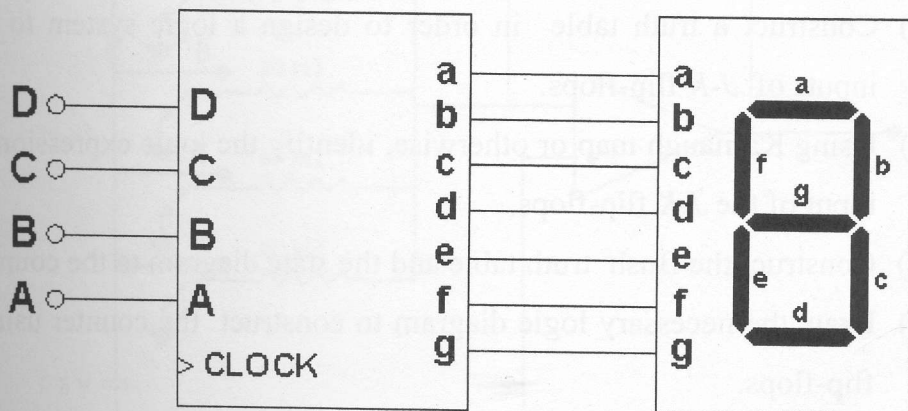
where A_0 and R_i are the open loop gain and the open loop input resistance of the operational amplifier respectively and B is the feedback fraction.

- (v) Calculate the voltage gain A_f and the input resistance R_f if $R_1 = 100 \text{ k}\Omega$, $R_2 = 1 \text{ k}\Omega$, $A_0 = 100,000$ and $R_i = 2 \text{ M}\Omega$.

Discuss the features of the non-inverting operational amplifier given below.



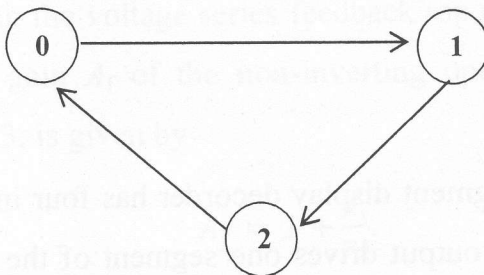
A BCD to seven-segment display decoder has four inputs (A, B, C and D) and seven outputs. Each output drives one segment of the display. A logic 1 output causes the segment to be lit.



- Establish a truth table for the decoder outputs that display the decimal numbers 0,1,2.....9. Here, 'A' and 'D' refer the least significant digit and the most significant digit of the decoder respectively.
- Using a four variable Karnaugh map, obtain the minimized logic sum of product expression to illuminate the segment 'b'.
- Realize the logic expression using only NAND gates.

Q5. Draw the logic symbol and the truth table for the output of a $J-K$ flip-flop.

A ripple counter to the following state diagram is to be designed using $J-K$ flops.



- State how many $J-K$ flip-flops are required to design the counter.
- Construct a truth table in order to design a logic system to feed inputs of $J-K$ flip-flops.
- Using Karnaugh map or otherwise, identify the logic expressions for input of the $J-K$ flip-flops.
- Construct the Bush truth table and the state diagram to the counter.
- Draw the necessary logic diagram to construct the counter using flip-flops.

You may find the following state transition table useful.

	0→0	0→1	1→0	1→1
J	0	1	X	X
K	X	X	1	0

- (i) Briefly explain what is meant by 'Resolution' of Analogue/Digital conversion and also, write down an equation for the percent resolution of it.
- (ii) Determine the percent resolution of a five-bit digital to analogue (D/A) converter.
- (iii) The weighted resistor network of a summing network and amplifier of a digital to analogue converter is given below. Construct a table of analogue output level corresponding to all possible binary input quantities 0000 through 1111.

